single capacitor memory structures (i.e., a DRAM cell) can be interconnected with large grain copper based alloy metallurgy.

## EXAMPLE 6

This example shows Cu and its alloys surrounded at least on three sides by thin amorphous barrier layer. As the line width decreases, the liner or barrier thickness needs to be reduced. Otherwise, the liner occupies a large cross-sectional area of the trench to be filled with metal and thereby reducing the effective area and increasing the metal resistance. To remedy the problem, a thinnest possible liner made of amorphous material, e.g., W—Si—N or Ta—Si—N may be utilized. This is shown in FIG. **7** in a dual damascene structure, and in FIG. **8** in a single damascene structure. The liner **90** may include microcrystalline nitrides or carbides of W, Ta, Ti surrounded by an amorphous $Si_3N_4$ layer. To demonstrate this embodiment, nitrides of W were chosen.

In the process, a very thin W—Si—N is first deposited by the reaction of $NH_3$, $SiH_4$ and $WF_6$ at a reaction temperature between about 300° C. and about 400° C. The resultant structure showed amorphous nitride surrounding microcrystalline W—N. The resistivities achieved were determined to be between 100–200 $\mu\Omega$-cm. The structure does not have large grain boundaries and is useful as a good diffusion barrier for copper for temperatures up to 500° C. for 1 hour. The same structure can be produced by alternating reactions of $WF_6$+$SiH_4$ followed by $NH_3$ reaction in-situ and repeating the reaction of $WF_6$+$SiH_4$ until the desired film thickness is achieved.

Similarly, other techniques such as sputtering (i.e., a collimated, low/high pressure, ionized sputtering) and composite sputtering targets (e.g., Ta—Si—N) may be used to achieve the same barrier materials. A film layer of large grain Cu is then deposited on top of the barrier material. Using the prescribed relationship for damascene, Cu can be removed from the amorphous liner. Utilizing the difference in rate for large grain Cu and small grain liner, a good selectivity in polishing between liner and Cu can be achieved. Another slurry can be used to remove the amorphous liner from the top of the dielectric.

Another structure using single damascene technique can be created by the present invention. This is shown in FIG. **8**. In this structure, M2 level copper **100** is connected to M1 level copper **102** by a via **104** formed on two stages. First, via **104** is formed on top of M1 layer **102** metal (e.g., W, large grain Al, Ag, Cu or their alloys) can be deposited in via **104** within a diffusion barrier layer and then polished off. Then forming trenches into oxide lines on top of the via. By depositing large grain copper and then polishing off, single damascene structure can be created. The advantage here is if the aspect ratios of vias and lines increase then single damascene would help to fill such stringent topography incrementally.

## EXAMPLE 7

In this example, efforts were made to further improve the performance of large grain Cu structure. A hard dielectric layer formed by a fluorinated oxide or nitride may be used in which copper lines with the liners discussed above can be formed in a dual damascene structure (see FIG. **2**). In addition, other dielectric materials such as an amorphous or porous oxide treated with silane or methane can also be used to lower the dielectric constant.

While the present invention has been described in an illustrative manner, it should be understood that the terminology used is intended to be in the nature of words of description rather than of limitation.



It is to be noted that the structure disclosed in this invention, i.e., dual damascene, single damascene, or structures formed with RIE can be repeated to form multilevel interconnect structure.

Furthermore, while the present invention has been described in terms of several preferred embodiments thereof, it is to be appreciated that those skilled in the art will readily apply these teachings to other possible variations of the invention.

The embodiments of the invention in which an exclusive property or privilege are claimed are defined as follows:

What is claim is:

**1**. A soft metal conductor for use in a semiconductor device comprising grains having grain sizes larger than 200 nm so as to provide a substantially scratch-free surface upon polishing in a subsequent chemical mechanical polishing step, said soft metal conductor being formed by at least one metal selected from the group consisting of Al, Cu and Ag.

**2**. An electrically conducting soft metal structure for use in a semiconductor device comprising:

an uppermost layer consisting of grains having grain sizes not smaller than 200 nm, and

a second layer contiguous with and immediately adjacent to said uppermost layer consisting of grains having grain sizes not larger than about 20% of the thickness of said soft metal structure.

**3**. An electrically conducting soft metal structure according to claim **2**, wherein said uppermost layer having a thickness sufficiently large to provide a substantially scratch-free and erosion-free surface upon polishing in a chemical mechanical polishing method.

**4**. An electrically conducting soft metal structure according to claim **2**, wherein said structure being made of a metal selected from the group consisting of aluminum, copper, silver, ternary and binary alloys of aluminum, copper, silver and any other low resistance metal.

**5**. An electrically conducting soft metal structure according to claim **2**, wherein said structure being a member selected from the group consisting of a via, an interconnect and a line.

**6**. An electrically conducting soft metal structure according to claim **2**, wherein said uppermost layer having grains of metal not less than 200 nm in grain size and a thickness of at least 100 nm.

**7**. An electrically conducting soft metal structure according to claim **2**, wherein said uppermost layer having grains of metal not less than 200 nm in grain size and said second layer having grains of metal not more than 100 nm in grain size.

**8**. An electrically conducting soft metal structure according to claim **2**, wherein said second layer having grains of metal not more than 100 nm in grain size and a thickness of not less than 600 nm.

**9**. An electrically conducting soft metal structure according to claim **2** further comprising a bottom layer contiguous with and immediately adjacent to said second layer, said bottom layer consisting of grain of metal not less than 200 nm in grain size.

**10**. A soft metal conductor for use in a semiconductor device comprising:

a first soft metal layer;

a Ti layer of less than 30 nm thick on top of said first metal layer;

a second soft metal layer on top of said Ti layer having in its uppermost surface metal grains of grain sizes not

smaller than about 20% of the thickness of said second metal layer, said first soft metal layer and said second soft metal layer are formed by at least one metal selected from the group consisting of Al, Cu and Ag; and

whereby said Ti layer sandwiched between two soft metal layers is converted to $TiAl_3$ upon annealing at a temperature higher than room temperature such that diffusion of atoms of said metal through said Ti $Al_3$ film occurs upon the passage of an electrical current therethrough and thus improving the electromigration resistance of said soft metal conductor.

**11**. A soft metal conductor according to claim **10**, wherein said first soft metal is formed by a member selected from the group consisting of Al, Cu, Ag, CuAg, CuAl, AgAl and CuAgAl.

**12**. A soft metal conductor according to claim **10**, wherein said Ti layer further comprising composite layers of Ti and Ti alloys including Ti/TiN.

**13**. A soft metal conductor according to claim **10**, wherein said Ti layer is situated at the bottom of a via having portions



of said layer in extremely small thickness or portions of said layer in voids so as to allow the existence of a continuous phase of said metal material or diffusion of said metal atoms across a $TiAl_3$ layer subsequently formed and a resulting improvement in the electromigration resistance of said soft metal conductor.

**14**. A soft metal conductor according to claim **10** further comprising an annealing step at a predetermined temperature and for a predetermined length of time sufficient to convert said Ti layer to $TiAl_3$ when said soft metal used in forming said first soft metal layer and said second soft metal layer is Al or AlCu.

**15**. A soft metal conductor according to claim **14**, wherein said predetermined temperature is not less than 300° C. and said predetermined length of time is not less than 10 min.

**16**. A soft metal conductor according to claim **14**, wherein said predetermined temperature is 400° C. and said predetermined length of time is 30 min.

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